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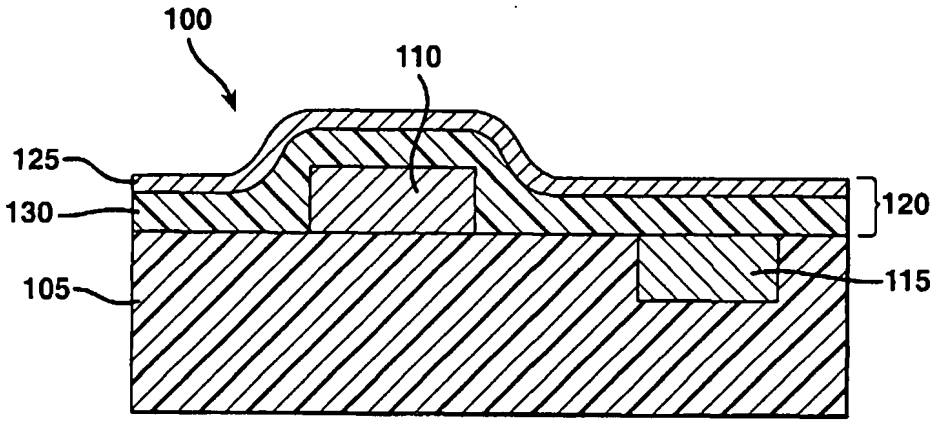

(57) Abstract: An encapsulated microelectronic device. The device includes a semiconductor substrate, microelectronic device adjacent to the semiconductor substrate, and at least one first barrier stack adjacent to the microelectronic device. The barrier stack encapsulates the microelectronic device. It includes at least one first barrier layer and at least one first polymer layer. The encapsulated microelectronic device optionally includes at least one second barrier stack located between the semiconductor substrate and the microelectronic device. The second barrier stack includes at least one second barrier layer and at least one second polymer layer. A method for making an encapsulated microelectronic device is also disclosed.

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ENCAPSULATED MICROELECTRONIC DEVICES

The present invention relates generally to microelectronic devices, and more particularly to microelectronic devices encapsulated in barrier stacks.

Microelectronic devices fabricated on semiconductor substrates require passivation, or encapsulation, to protect them from atmospheric contaminants and constituents, mechanical damage, stress, thermal stress and cycling, downstream processing, and corrosive chemicals.

Passivation of the microelectronic devices performs several functions. First, it electrically insulates the microelectronic device from other microelectronic devices. It preserves the recombination velocity at the semiconductor surface. It is also a stress buffer to minimize cracking. It provides protection from processing chemicals, ultraviolet light exposure, and photoresists during lithography processes. In addition, it provides protection from humidity, oxidants, corrosive materials, scratching, and mechanical damage. Finally, it provides gettering of mobile ions, such as Cl^-, and Na^+. Lavinger et al., J. Vac. Sci. Technol. A16(2), Mar./Apr. 1998, p. 530.

Conventional hermetic sealing in metal or ceramic provides effective protection. However, conventional hermetic enclosures are relatively bulky (about 4-6 mm deep), and they add a significant amount of weight to the product, which reduces the benefits of miniaturization.

Many devices that require passivation are now fabricated on glass, fused silica, and ceramic substrates. For example, thin films of amorphous silicon nitride (Si_3N_4) and silicon dioxide (SiO_2) are used on p-type semiconductor devices as a protective coating, a mask for lithography processes, charge storage systems in nonvolatile metal-nitride-oxide-semiconductor memory devices, insulators between metal layers, gate insulators for thin film transistors, and ultrathin dielectrics for very large scale integration devices. For integrated circuit applications, SiO_2 is the stress buffer layer and Si_3N_4 is the passivation layer, as described in U.S. Patent No. 5,851,603, which is incorporated herein by reference. Silicon nitride is primarily deposited by chemical vapor deposition processes (CVD), such as atmospheric pressure chemical vapor deposition (APCVD), low pressure chemical vapor

deposition (LPCVD), and plasma enhanced chemical vapor deposition (PECVD). However, the use of inorganic materials deposited by standard semiconductor processes such as chemical vapor deposition has several disadvantages. The most serious disadvantages are brittleness, a tendency to crack under mechanical stress, poor step coverage, poor planarization properties, and poor barrier properties. The best oxygen permeation rate for Si_3N_4 deposited by electron cyclotron resonance-plasma enhanced vapor deposition (ECR PECVD) is reported to be near 1 $cc/m^2/day$. The best oxygen permeation rate for SiO_2 is also near 1 $cc/m^2/day$.

As a result of these problems, there has been a significant effort to replace inorganic materials such as SiO_2 and Si_3N_4 with polymer dielectrics. Polymer materials of interest include polyimide, polyamide, and paralyene. Organic materials offer good adhesion, sufficient elasticity, and sufficient tensile strength. However, these materials have problems with brittleness and defects such as voids. C.P. Wong, Ceramic Trans. 33, 1993 p. 125.

The barrier protection offered by inorganic and organic materials is not usually adequate to ensure reliable microelectronic device operation. Additional barrier layers are added prior to encapsulation. Materials such as silicon rubber are used as barriers. The integrated circuit can be embedded in plastic by injection molding to add further moisture barrier protection.

Epoxies are also used for barrier applications and encapsulation. The epoxy layers used for encapsulation are only about one quarter of the thickness of the layers required for convention hermetic sealing. However, even that thickness produces a device which is unacceptably heavy and bulky in many applications. In addition, epoxies have a water vapor permeation rate which is too high for some applications.

The passivation layers currently being used in microelectronics include silicon dioxide, silicon nitride, and silicon oxynitride layers with thicknesses up to about 1μm. These layers are deposited by CVD and reactive magnetron sputtering processes, which can require substrate and processing temperatures as high as

800°C. Materials deposited by CVD can also have very stresses (i.e., greater than 10,000 MPa).

The inorganic layer is often followed by a spin cast polyimide layer about 0.5 μm thick. The polyimide layer is used for passivation, encapsulation, planarization, and bonding/molding to the packaging. The layer is spun on and cured at temperatures up to 250°C. The oxygen and water vapor barrier properties of polyimide are poor and typical of polymer substrates (>10 cc/m^2/day). Polyimide is very opaque and strongly absorbing at visible wavelengths. Polyimide films can have large numbers of voids, which can cause reliability problems with integrated circuits. The voids can also cause hot spots and cracks that can damage integrated circuit components.

Another method used to protect microelectronic circuitry is vapor deposition of a thin film of parylene. However, the water vapor permeation rate of the parylene is too high for many applications. In addition, parylene is subject to thermal oxidation at temperatures over about 120°C.

Furthermore, PECVD coatings have problems with pinholes, poor step coverage, and particulates. The quality of the coating is usually poor. Deposition processes for these layers can damage temperature sensitive material in, for example, integrated circuits, organic light emitting devices, light emitting polymers and microlasers. As a result, totally effective encapsulation of temperature sensitive devices cannot be achieved on semiconductor substrates using conventional deposition processes. Additionally, in order to obtain the required encapsulation and passivation, the current passivation layers must be thick compared to device thicknesses and sizes, which causes problems in the fabrication of multilevel integrated circuits. Finally, as discussed above, the barrier properties for these materials are inadequate for many applications.

Thus, there is a need for an improved, lightweight, thin film, barrier construction which can be used to encapsulate microelectronic devices, and for methods for making such encapsulated microelectronic devices.

The present invention meets these needs by providing an encapsulated microelectronic device and a method for making such a device. The device includes a semiconductor substrate, a microelectronic device adjacent to the semiconductor substrate, and at least one first barrier stack adjacent to the microelectronic device. By adjacent, we mean next to, but not necessarily directly next to. There can be additional intervening layers. The barrier stack encapsulates the microelectronic device. It includes at least one first barrier layer and at least one first polymer layer. The encapsulated microelectronic device optionally includes at least one second barrier stack located between the semiconductor substrate and the microelectronic device. The second barrier stack includes at least one second barrier layer and at least one second polymer layer.

Preferably, either one or both of the first and second barrier layers of the first and second barrier stacks is substantially transparent. At least one of the first barrier layers preferably comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof.

Either one of the first and second barrier layers can be substantially opaque, if desired. The opaque barrier layers are preferably selected from opaque metals, opaque polymers, opaque ceramics, and opaque cermets.

The polymer layers of the first and second barrier stacks are preferably acrylate-containing polymers. As used herein, the term acrylate-containing polymers includes acrylate-containing polymers, methacrylate-containing polymers, and combinations thereof. The polymer layers in the first and/or the second barrier stacks can be the same or different.

The semiconductor substrate can either be flexible or rigid.

The microelectronic device is preferably selected from integrated circuits, charge coupled devices, light emitting diodes, light emitting polymers, organic light emitting devices, metal sensor pads, micro-disk lasers, electrochromic devices, photochromic devices, microelectromechanical systems, and solar cells.

The encapsulated microelectronic device can include additional layers if desired, such as polymer smoothing layers, scratch resistant layers, or other functional layers. The encapsulated microelectronic device can also include a lid adjacent to the at least one first barrier stack.

The present invention also involves a method of making the encapsulated microelectronic device. The method includes providing a semiconductor substrate having an microelectronic device thereon, and placing at least one first barrier stack over the microelectronic device to encapsulate the microelectronic device. The barrier stack includes at least one first barrier layer and at least one first polymer layer.

The microelectronic device can be placed on the semiconductor substrate by diffusion, ion implantation on deposition, or lamination. The at least one first barrier stack can be placed over the microelectronic device by deposition, preferably vacuum deposition, or by laminating the barrier stack over the environmentally sensitive device. The lamination can be performed using an adhesive, solder, ultrasonic welding, pressure, or heat.

A second barrier stack can be placed on the semiconductor substrate before the microelectronic device is placed there. The second barrier stack includes at least one second barrier layer and at least one second polymer layer. The second barrier stack can be deposited on the semiconductor substrate, preferably by vacuum deposition.

The semiconductor substrate can be removed from the encapsulated microelectronic device, if desired.

Accordingly, it is an object of the present invention to provide an encapsulated microelectronic device, and to provide a method of making such as device.

Fig. 1 is a cross-section of one embodiment of the encapsulated microelectronic device of the present invention.

Fig. 2 is a cross-section of a second embodiment of the encapsulated microelectronic device of the present invention.

One embodiment of the encapsulated microelectronic device of the present invention is shown in Fig. 1. The encapsulated microelectronic device 100 includes a semiconductor substrate 105, microelectronic devices 110 and 115, and a first barrier stack 120. Microelectronic device 115 is embedded in semiconductor substrate 105. Microelectronic device 110 is placed on the semiconductor substrate 105. The first barrier stack 120 includes at least one first barrier layer 125 and at least one first polymer layer 130. The first barrier stack 120 encapsulates and passivates the microelectronic devices 110 and 115.

The semiconductor substrate 105 can be either rigid or flexible.

Examples of microelectronic devices 110 and 115 include, but are not limited to, integrated circuits, charge coupled devices, light emitting diodes, light emitting polymers, organic light emitting devices, metal sensor pads, micro-disk lasers, electrochromic devices, photochromic devices, microelectromechanical systems and solar cells. These microelectronic devices can be made using known techniques, such as those described in U.S. Patent Nos. 6,043,523 and 6,030,852 (charged couple devices); U.S. Patent Nos. 6,040,588 and 6,067,188 (LEDs); U.S. Patent Nos. 6,023,373, 6,023,124, 6,023,125 (LEPs); U.S. Patent Nos. 5,629,389, 5,747,182, 5,844,363, 5,872,355, 5,902,688, and 5,948,552 (OLEDs); Martin, et al.; Fabrication of Plastic Microfluidic Components, SPIE Proceedings 3515, 1998, 177; Matson, et al., Fabrication Processes for Polymer-Based Microfluidic Analytical Devices, Proceedings of μ-TAS '98, 1998, (metal sensor pads), U.S. Patent Nos. 5,825,799 and 5,790,582 (micro-disk lasers); U.S. Patent Nos. 5,995,273, 5,888,431, and 4,253,741 (electrochromic devices); U.S. Patent Nos. 4,838,483 and 5,604,626 (photochromic devices); U.S. Patent Nos. 5,761,350 and 6,046,066 (microelectromechanical systems); and M. Sittig, Solar Cells for Photovoltaic Generation of Electricity, Energy Technology Review, No. 48, Noyes Data Corp. NY 1979 (solar cells) which are incorporated herein by reference.

In each barrier stack 120, there can be one or more barrier layers 125 and one or more polymer layers 130. The barrier layers and polymer layers in the barrier stack can be made of the same material or of a different material. The barrier layers

are typically about 100-400 Å thick, and the polymer layers are typically about 1000-10,000 Å thick.

Although Fig. 1 shows a barrier stack with a single barrier layer and a single polymer layer, the barrier stacks can have one or more polymer layers and one or more barrier layers. There could be one polymer layer and one barrier layer, there could be one or more polymer layers on one side of one or more barrier layers, or there could be one or more polymer layers on both sides of one or more barrier layers. The important feature is that the barrier stack have at least one polymer layer and at least one barrier layer.

There can be additional overcoat layers on top of the barrier stack, such as organic or inorganic layers, planarizing layers, transparent conductors, antireflective coatings, or other functional layers, if desired.

Optionally, the semiconductor substrate can be placed on a plastic substrate. In this case, a barrier stack is preferably placed on the plastic substrate before the semiconductor substrate is placed thereon.

A second embodiment of the encapsulated microelectronic device of the present invention is shown in Fig. 2. The encapsulated microelectronic device 200 has a semiconductor substrate 205. There are scratch resistant layers 210 on either side of the semiconductor substrate 205 to protect it. When a scratch resistant layer is included, it is preferred that both sides of the semiconductor substrate have a scratch resistant layer. This helps to prevent curling of a flexible semiconductor substrate.

On top of the scratch resistant layer 210, there is a polymer smoothing layer 215. The polymer smoothing layer, decreases surface roughness, and encapsulates surface defects, such as pits, scratches, and digs. This produces a planarized surface which is ideal for deposition of subsequent layers. Depending on the desired application, there can be additional layers deposited on the semiconductor substrate 205, such as organic or inorganic layers, planarizing layers, electrode layers, antireflective coatings and other functional layers. In this way, the semiconductor substrate can be specifically tailored to different applications.

The first barrier stack 220 is above the polymer smoothing layer 215. The first barrier stack 220 includes a first barrier layer 225 and a first polymer layer 230. The first barrier layer 225 includes barrier layers 235 and 240. Barrier layers 235 and 240 can be made of the same barrier material or of different barrier materials.

There are microelectronic devices 245 and 250. Microelectronic device 245 is embedded in substrate 205. Microelectronic device 250 is placed over the first barrier stack 220. There is a second barrier stack 255 placed over the microelectronic device 250 to encapsulate it. The second barrier stack 255 has a barrier layer 260 and a polymer layer 265, although it can have one or more barrier layers and one or more polymer layers, as discussed above. The barrier layers and polymer layers in the first and second barrier stacks can be the same or they can be different. Although only one first barrier stack and only one second barrier stack are shown in Fig. 2, the number of barrier stacks is not limited. The number of barrier stacks needed depends on the semiconductor substrate material used and the level of water vapor and oxygen permeation resistance needed for the particular application. One or two barrier stacks should provide sufficient barrier properties for some applications. The most stringent applications may require five or more barrier stacks.

There is a lid 270 over the second barrier stack 255. The lid can be can be either rigid or flexible. A flexible lid can be made of any flexible material including, but not limited to: polymers, for example, polyethylene terephthalate (PET), polyethylene naphthalate (PEN), or high temperature polymers such as polyether sulfone (PES), polyimides, or Transphan™ (a high glass transition temperature cyclic olefin polymer available from Lofo High Tech Film, GMBH of Weil am Rhein, Germany); metal; paper; fabric; and combinations thereof. Rigid lids are preferably made of glass, metal, or semiconductors.

The method of making the encapsulated microelectronic device will be described with reference to the embodiment shown in Fig. 2. A microelectronic device can be embedded in the semiconductor substrate by diffusion and ion implantation. Any initial layers which are desired, such as scratch resistant layers,

planarizing layers, electrically conductive layers, etc., can be coated, deposited, or otherwise placed on the semiconductor substrate. A polymer smoothing layer is preferably included to provide a smooth base for the remaining layers. It can be formed by depositing a layer of polymer, for example, an acrylate-containing polymer, onto the semiconductor substrate or previous layer. The polymer layer can be deposited in vacuum or by using atmospheric processes such as spin coating and/or spraying. Preferably, an acrylate-containing monomer, oligomer, or resin is deposited and then polymerized *in situ* to form the polymer layer. As used herein, the term acrylate-containing monomer, oligomer, or resin includes acrylate-containing monomers, oligomers, and resins, methacrylate-containing monomers, oligomers, and resins, and combinations thereof.

The first barrier stack is then placed on the semiconductor substrate. The first and second barrier stacks include at least one barrier layer and at least one polymer layer. The barrier stacks are preferably made by vacuum deposition. The barrier layer can be vacuum deposited onto the polymer smoothing layer, semiconductor substrate, or previous layer. The polymer layer is then deposited on the barrier layer, preferably by flash evaporating acrylate-containing monomers, oligomers, or resins, condensing on the barrier layer, and polymerizing *in situ* in a vacuum chamber. U.S. Patent Nos. 5,440,446 and 5,725,909, which are incorporated herein by reference, describe methods of depositing thin film, barrier stacks.

Vacuum deposition includes flash evaporation of acrylate-containing monomer, oligomer, or resin with *in situ* polymerization under vacuum, plasma deposition and polymerization of acrylate-containing monomer, oligomer, or resin, as well as vacuum deposition of the barrier layers by sputtering, chemical vapor deposition, plasma enhanced chemical vapor deposition, evaporation, sublimation, electron cyclotron resonance-plasma enhanced vapor deposition (ECR-PECVD), and combinations thereof.

In order to protect the integrity of the barrier layer, the formation of defects and/or microcracks in the deposited layer subsequent to deposition and prior to

downstream processing should be avoided. The encapsulated microelectronic device is preferably manufactured so that the barrier layers are not directly contacted by any equipment, such as rollers in a web coating system, to avoid defects that may be caused by abrasion over a roll or roller. This can be accomplished by designing the deposition system such that the barrier layers are always covered by polymer layers prior to contacting or touching any handling equipment.

Another microelectronic device is then placed on the first barrier layer. The microelectronic device can be placed on the semiconductor substrate by deposition, diffusion, ion implantation, or lamination. The deposition can be vacuum deposition. The lamination can use an adhesive, such as glue, or the like, solder, ultrasonic welding, pressure, or heat to seal the microelectronic device to the semiconductor substrate.

The second barrier stack is then placed over the microelectronic device to encapsulate it. The second barrier stack can be placed over the microelectronic device by deposition or lamination.

The barrier layers in the first and second barrier stacks may be any barrier material. The barrier layers in the first and second barrier stacks can be made of the same material or a different material. In addition, multiple barrier layers of the same or different barrier materials can be used in a barrier stack.

The barrier layers can be transparent or opaque, depending on the design and application of the microelectronic device. Preferred transparent barrier materials include, but are not limited to, metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof. The metal oxides are preferably selected from silicon oxide, aluminum oxide, titanium oxide, indium oxide, tin oxide, indium tin oxide, tantalum oxide, zirconium oxide, niobium oxide, and combinations thereof. The metal nitrides are preferably selected from aluminum nitride, silicon nitride, boron nitride, and combinations thereof. The metal oxynitrides are preferably selected from aluminum oxynitride, silicon oxynitride, boron oxynitride, and combinations thereof.

Opaque barrier layers can be used in some barrier stacks depending on the design of the microelectronic device. Opaque barrier materials include, but are not limited to, metals, ceramics, polymers, or cermets. Examples of opaque cermets include, but are not limited to, zirconium nitride, titanium nitride, hafnium nitride, tantalum nitride, niobium nitride, tungsten disilicide, titanium diboride, and zirconium diboride.

The polymer layers of the first and second barrier stacks are preferably acrylate-containing monomers, oligomers, or resins. The polymer layers in the first and second barrier stacks can be the same or different. In addition, the polymer layers within each barrier stack can be the same or different.

Because the encapsulation/barrier stacks can be transparent layers with different dielectric constants, refractive index, and extinction coefficients, optical interference in the layers can be employed to add functionality to the coating. By adjusting layer thicknesses, the coating can be designed to perform antireflection, bandpass, notch filter, dichroic, and high reflection functions, thus controlling the light intensity and wavelengths into and out of the device. This can be useful for optical sensor devices such as organic light emitting devices, microlasers, light emitting polymers, and light emitting diodes.

In a preferred embodiment, the barrier stack includes a polymer layer and two barrier layers. The two barrier layers can be made from the same barrier material or from different barrier materials. The thickness of each barrier layer in this embodiment is about one half the thickness of the single barrier layer, or about 100 to 150 Å. There are no limitations on the thickness, however.

When the barrier layers are made of the same material, they can be deposited either by sequential deposition using two sources or by the same source using two passes. If two deposition sources are used, deposition conditions can be different for each source, leading to differences in microstructure and defect dimensions. Any type of deposition source can be used. Different types of deposition processes, such as magnetron sputtering and electron beam evaporation, can be used to deposit the two barrier layers.

The microstructures of the two barrier layers are mismatched as a result of the differing deposition sources/parameters. The barrier layers can even have different crystal structure. For example, Al_2O_3 can exist in different phases (alpha, gamma) with different crystal orientations. The mismatched microstructure can help decouple defects in the adjacent barrier layers, enhancing the tortuous path for gases and water vapor permeation.

When the barrier layers are made of different materials, two deposition sources are needed. This can be accomplished by a variety of techniques. For example, if the materials are deposited by sputtering, sputtering targets of different compositions could be used to obtain thin films of different compositions. Alternatively, two sputtering targets of the same composition could be used but with different reactive gases. Two different types of deposition sources could also be used. In this arrangement, the lattices of the two layers are even more mismatched by the different microstructures and lattice parameters of the two materials.

A single pass, roll-to-roll, vacuum deposition of a three layer combination on a PET substrate, i.e., PET substrate/polymer layer/barrier layer/polymer layer, can be more than five orders of magnitude less permeable to oxygen and water vapor than a single oxide layer on PET alone. See J.D. Affinity, M.E. Gross, C.A.Coronado, G.L. Graff, EN Greenwell, and P.M. Martin, Polymer-Oxide Transparent Barrier Layers Produced Using PAL Process, 39th Annual Technical Conference Proceedings of the Society of Vacuum Caters, Vacuum Web Coating Session, 1996, pages 392-397; J.D.Affinito, S. Eufinger, M.E.Gross, G.L.Graff, and P.M. Martin, PAL/Oxide/PAL Barrier Layer Performance Differences Arising From Use of UV or Electron Beam Polymerization of the PAL Layers, Thin Solid Films, Vol.308, 1997, pages 19-25. This is in spite of the fact that the effect on the permeation rate of the polymer multilayers (PAL) layers alone, without the barrier layer (oxide, metal, nitride, oxynitride) layer, is barely measurable. It is believed that the improvement in barrier properties is due to two factors. First, permeation rates in the roll-to-roll coated oxide-only layers were found to be conductance limited by defects in the oxide layer that arose during deposition and when the coated substrate was wound

up over system idlers/rollers. Asperities (high points) in the underlying substrate are replicated in the deposited inorganic barrier layer. These features are subject to mechanical damage during web handling/take-up, and can lead to the formation of defects in the deposited film. These defects seriously limit the ultimate barrier performance of the films. In the single pass, polymer/barrier/polymer process, the first acrylic layer planarizes the substrate and provides an ideal surface for subsequent deposition of the inorganic barrier thin film. The second polymer layer provides a robust "protective" film that minimizes damage to the barrier layer and also planarizes the structure for subsequent barrier layer (or microelectronic device) deposition. The intermediate polymer layers also decouple defects that exist in adjacent inorganic barrier layers, thus creating a tortuous path for gas diffusion.

The permeability of the barrier stacks used in the present invention is shown in Table 1. The barrier stacks of the present invention on polymeric substrates, such as PET, have measured oxygen transmission rates (OTR) and water vapor transmission rates (WVTR) values well below the detection limits of current industrial instrumentation used for permeation measurements (Mocon OxTran 2/20L and Permatran). Table 1 shows the OTR and WVTR values (measured according to ASTM F 1927-98 and ASTM 1249-90, respectively) measured at Mocon (Minneapolis, MN) for several barrier stacks on 7 mil PET along with reported values for other materials.

Table 1

Sample	Oxygen Permeation Rate ($cc/m^2/day$)		Water Vapor Permeation ($g/m^2/day$)+	
	23°C	38°C	23°C	38°C
Native 7 mil PET	7.62	-	-	-
1-barrier stack	<0.005	<0.005*	-	0.46+
1-barrier stack with ITO	<0.005	<0.005*	-	0.011+
2-barrier stacks	<0.005	<0.005*	-	<0.005+
2-barrier stacks with ITO	<0.005	<0.005*	-	<0.005+
5-barrier stacks	<0.005	<0.005*	-	<0.005+
5-barrier stacks with ITO	<0.005	<0.005*	-	<0.005+
DuPont film [1] (PET/Si_3N_4 or PEN/Si_3N_4)	0.3	-	-	-
Polaroid film [1]	<1.0	-	-	-
PET/Al[2]	0.6	-	0.17	-
PET/silicon oxide[2]	0.7 – 1.5	-	0.15 – 0.9	-
Teijin LCD film (HA grade - TN/STN)[3]	<2	-	<5	-

(*) 38°C, 90% RH, 100% O_2

(+) 38°C, 100% RH

1 - P.F. Carcia, 46th International Symposium of the American Vacuum Society, Oct. 1999

2 - Langowski, H.C., 39th Annual Technical Conference Proceedings, SVC, pp. 398-401 (1996)

3 - Technical Data Sheets

As the data in Table 1 shows, the barrier stacks of the present invention provide oxygen and water vapor permeation rates several orders of magnitude better than PET coated with aluminum, silicon oxide, or aluminum oxide. The barrier stacks are extremely effective in preventing oxygen and water penetration to the underlying components, substantially outperforming other barrier coatings on the market. The barrier stacks have an oxygen transmission rate of less than 0.005 $cc/m^2/day$ at 23°C and 0% relative humidity, an oxygen transmission rate of less than 0.005 $cc/m^2/day$ at 38°C and 90% relative humidity, and a water vapor transmission rate of less than 0.005 $g/m^2/day$ at 38°C and 100% relative humidity. The actual transmission rates of the barrier stacks is less than this, but it cannot be measured with existing equipment.

Semiconductor passivation is compatible with flexible and rigid semiconductor substrates. The barrier stacks can be deposited in a batch, in-line or cluster tool, or on thin film transistors deposited on flexible substrates, such as metal foils and polymeric webs. The encapsulation/barrier stack deposition process is compatible with integrated circuit fabrication processes and does not damage sensitive microcircuitry and active devices. The barrier stacks can be deposited over nonuniform surfaces and can effectively encapsulate and planarize surface features.

Because the preferred process involves flash evaporation of a monomer and magnetron sputtering, deposition temperatures are below 100°C, which is much less than the 300°C to 800°C temperatures required for CVD coating processes, and stresses in the coating can be minimized. Because of the low temperatures, the process does not harm or degrade temperature sensitive components. Multilayer coatings can be deposited at high deposition rates. No harsh gases or chemicals are used, and the process can be scaled up to large substrates and wide webs. The barrier properties of the coating can be tailored to the application by controlling the number of layers, the materials, and the layer design.

The encapsulation process of the present invention provides improved encapsulation of microelectronic devices on semiconductor substrates. In addition to the improved barrier properties, the chemical resistance, thermal and shock resistance, mechanical robustness, and coating quality are also improved. As a result, the lifetime of the encapsulated microelectronic devices is significantly increased.

Thus, the present invention provides a barrier stack with the exceptional barrier and other properties necessary for hermetic sealing of an microelectronic device.

While certain representative embodiments and details have been shown for purposes of illustrating the invention, it will be apparent to those skilled in the art that various changes in the compositions and methods disclosed herein may be made without departing from the scope of the invention, which is defined in the appended claims.

CLAIMS

1. An encapsulated microelectronic device comprising:
a semiconductor substrate;
an microelectronic device adjacent to the semiconductor substrate; and
at least one first barrier stack comprising at least one first barrier layer and at least one first polymer layer, the at least one first barrier stack adjacent to the microelectronic device, wherein the at least one first barrier stack encapsulates the microelectronic device.

2. The encapsulated microelectronic device of claim 1 further comprising at least one second barrier stack located between the semiconductor substrate and the microelectronic device, the at least one second barrier stack comprising at least one second barrier layer and at least one second polymer layer.

3. The encapsulated microelectronic device of claim 1 wherein the at least one first barrier layer is substantially transparent.

4. The encapsulated microelectronic device of claim 2 wherein the at least one second barrier layer is substantially transparent.

5. The encapsulated microelectronic device of claim 1 wherein at least one of the at least one first barrier layers comprises a material selected from metal oxides, metal nitrides, metal carbides, metal oxynitrides, metal oxyborides, and combinations thereof.

6. The encapsulated microelectronic device of claim 5 wherein the metal oxides are selected from silicon oxide, aluminum oxide, titanium oxide, indium oxide, tin oxide, indium tin oxide, tantalum oxide, zirconium oxide, niobium oxide, and combinations thereof.

7. The encapsulated microelectronic device of claim 5 wherein the metal nitrides are selected from aluminum nitride, silicon nitride, boron nitride, and combinations thereof.

8. The encapsulated microelectronic device of claim 5 wherein the metal oxynitrides are selected from aluminum oxynitride, silicon oxynitride, boron oxynitride, and combinations thereof.

9. The encapsulated microelectronic device of claim 1 wherein the at least one first barrier layer is substantially opaque.

10. The encapsulated microelectronic device of claim 2 wherein the at least one second barrier layer is substantially opaque.

11. The encapsulated microelectronic device of claim 1 wherein at least one of the at least one first barrier layers is selected from opaque metals, opaque polymers, opaque ceramics, and opaque cermets.

12. The encapsulated microelectronic device of claim 2 wherein at least one of the at least one second barrier layers is selected from opaque metals, opaque polymers, opaque ceramics, and opaque cermets.

13. The encapsulated microelectronic device of claim 1 wherein the semiconductor substrate comprises a flexible semiconductor substrate material.

14. The encapsulated microelectronic device of claim 1 wherein the semiconductor substrate comprises a rigid semiconductor substrate material.

15. The encapsulated microelectronic device of claim 1 wherein at least one of the at least one first polymer layers comprises an acrylate-containing polymer.

16. The encapsulated microelectronic device of claim 2 wherein at least one of the at least one second polymer layers comprises an acrylate-containing polymer.

17. The encapsulated microelectronic device of claim 1 wherein the microelectronic device is selected from integrated circuits, charge coupled devices, light emitting diodes, light emitting polymers, organic light emitting devices, metal sensor pads, micro-disk lasers, electrochromic devices, photochromic devices, microelectromechanical systems and solar cells.

18. The encapsulated microelectronic device of claim 1 further comprising a polymer smoothing layer adjacent to the semiconductor substrate.

19. The encapsulated microelectronic device of claim 1 further comprising a scratch resistant layer adjacent to the semiconductor substrate.

20. The encapsulated microelectronic device of claim 1 further comprising an antireflective coating.

21. The encapsulated microelectronic device of claim 1 further comprising an antifingerprint coating.

22. The encapsulated microelectronic device of claim 1 further comprising an antistatic coating.

23. The encapsulated microelectronic device of claim 1 wherein the at least one first barrier layer comprises two barrier layers.

24. The encapsulated microelectronic device of claim 23 wherein the two barrier layers are made of the same barrier material.

25. The encapsulated microelectronic device of claim 23 wherein the two barrier layers are made of different barrier materials.

26. The encapsulated microelectronic device of claim 1 wherein the oxygen transmission rate through the at least one first barrier stack is less than 0.005 cc/m^2/day at 23°C and 0% relative humidity, and wherein the oxygen transmission rate through the at least one first barrier stack is less than 0.005 cc/m^2/day at 38°C and 90% relative humidity.

27. The encapsulated display device of claim 1 wherein the water vapor transmission rate through the at least one first barrier stack is less than 0.005 gm/m^2/day at 38°C and 100% relative humidity.

28. The encapsulated display device of claim 1 further comprising a plastic substrate adjacent to the semiconductor substrate on a side opposite the microelectronic device.

29. The encapsulate display device of claim 28 further comprising at least one third barrier stack located between the plastic substrate and the polymer substrate, the at least one third barrier stack comprising at least one third barrier layer and at least one third polymer layer.

30. The encapsulated microelectronic device of claim 1 further comprising a lid adjacent to the at least one first barrier stack.

31. The encapsulated microelectronic device of claim 1 wherein the microelectronic device is embedded in the semiconductor substrate.

32. An encapsulated microelectronic device comprising:

at least one first barrier stack comprising at least one first barrier layer and at least one first polymer layer;

an microelectronic device adjacent to the at least one first barrier stack; and

at least one second barrier stack comprising at least one second barrier layer and at least one second polymer layer, wherein the at least one first barrier stack and the at least one second barrier stack encapsulate the microelectronic device.

33. The encapsulated microelectronic device of claim 32 further comprising a semiconductor substrate adjacent to the at least one first barrier stack on a side opposite the microelectronic device.

34. A method of making an encapsulated microelectronic device comprising:

providing a semiconductor substrate having an microelectronic device thereon; and

placing at least one first barrier stack comprising at least one first barrier layer and at least one first polymer layer over the microelectronic device to encapsulate the microelectronic device.

35. The method of claim 34 wherein the step of placing the at least one first barrier stack over the microelectronic device comprises depositing the at least one first barrier stack over the microelectronic device.

36. The method of claim 35 wherein the at least one first barrier stack is vacuum deposited.

37. The method of claim 35 wherein the at least one first barrier layer is vacuum deposited and the at least one first polymer layer is deposited.

38. The method of claim 34 wherein the step of placing the at least one first barrier stack over the microelectronic device comprises laminating the at least one first barrier stack over the microelectronic device.

39. The method of claim 38 wherein the at least one first barrier stack is laminated using an adhesive.

40. The method of claim 38 wherein the at least one first barrier stack is laminated using heat.

41. The method of claim 34 wherein the step of providing the semiconductor substrate having the microelectronic device thereon comprises:
providing the semiconductor substrate; and
placing the microelectronic device on the semiconductor substrate.

42. The method of claim 41 wherein the step of placing the microelectronic device on the semiconductor substrate comprises depositing the microelectronic device on the semiconductor substrate.

43. The method of claim 42 wherein the microelectronic device is vacuum deposited.

44. The method of claim 41 wherein the step of placing the microelectronic device on the semiconductor substrate comprises laminating the microelectronic device on the semiconductor substrate.

45. The method of claim 41 wherein the step of placing the at least one first barrier stack over the microelectronic device comprises using diffusion to place the at least one first barrier stack over the microelectronic device.

46. The method of claim 41 wherein the step of placing the at least one first barrier stack over the microelectronic device comprises using ion implantation to place the at least one first barrier stack over the microelectronic device.

47. The method of claim 41 further comprising placing a second barrier stack comprising at least one second barrier layer and at least one second polymer layer on the semiconductor substrate before the microelectronic device is placed thereon.

48. The method of claim 47 wherein the step of placing the at least one second barrier stack on the semiconductor substrate comprises depositing the at least one second barrier stack on the semiconductor substrate.

49. The method of claim 48 wherein the at least one second barrier stack is vacuum deposited.

50. The method of claim 49 wherein the at least one second barrier layer is vacuum deposited and the at least one second polymer layer is deposited.

51. The method of claim 34 further comprising placing a lid over the at least one first barrier stack.

52. The method of claim 34 wherein the at least one first barrier layer comprises two barrier layers.

53. The method of claim 52 wherein the two barrier layers are deposited using the same deposition source.

54. The method of claim 52 wherein the two barrier layers are deposited using different deposition sources.

55. The method of claim 52 wherein the two barriers layers are vacuum deposited.

56. The method of claim 52 wherein the two barrier layers are made of the same barrier material.

57. The method of claim 52 wherein the two barrier layers are made of different barrier materials.

58. The method of claim 47 wherein the at least one second barrier layer comprises two barrier layers.

59. The method of claim 34 further comprising providing placing the semiconductor substrate on a polymer substrate.

60. The method of claim 59 further comprising placing at least one third barrier stack on the polymer substrate before the semiconductor is placed thereon, the at least one third barrier stack comprising at least one third barrier layer and at least one third polymer layer.

61. The method of claim 41 wherein the step of placing the microelectronic device on the semiconductor substrate comprises embedding the microelectronic device in the semiconductor substrate.

62. The method of claim 61 wherein the microelectronic device is embedded in the semiconductor substrate by diffusion.

63. The method of claim 61 wherein the microelectronic device is embedded in the semiconductor substrate by ion implantation.

FIG. 1

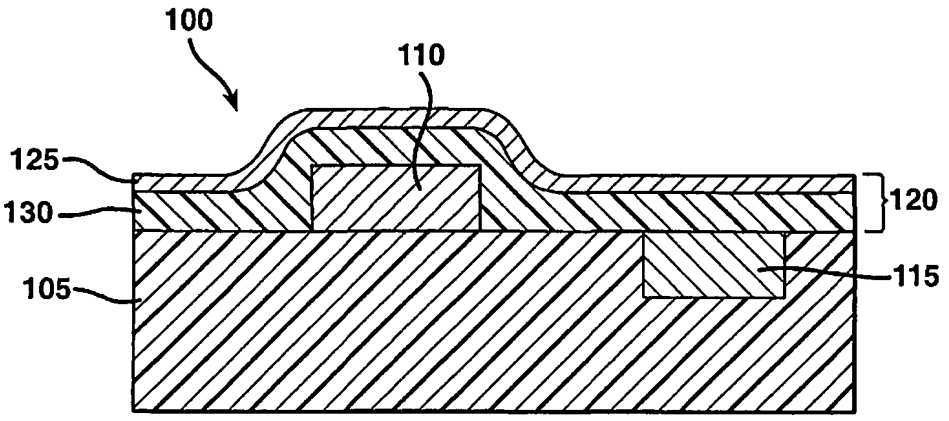
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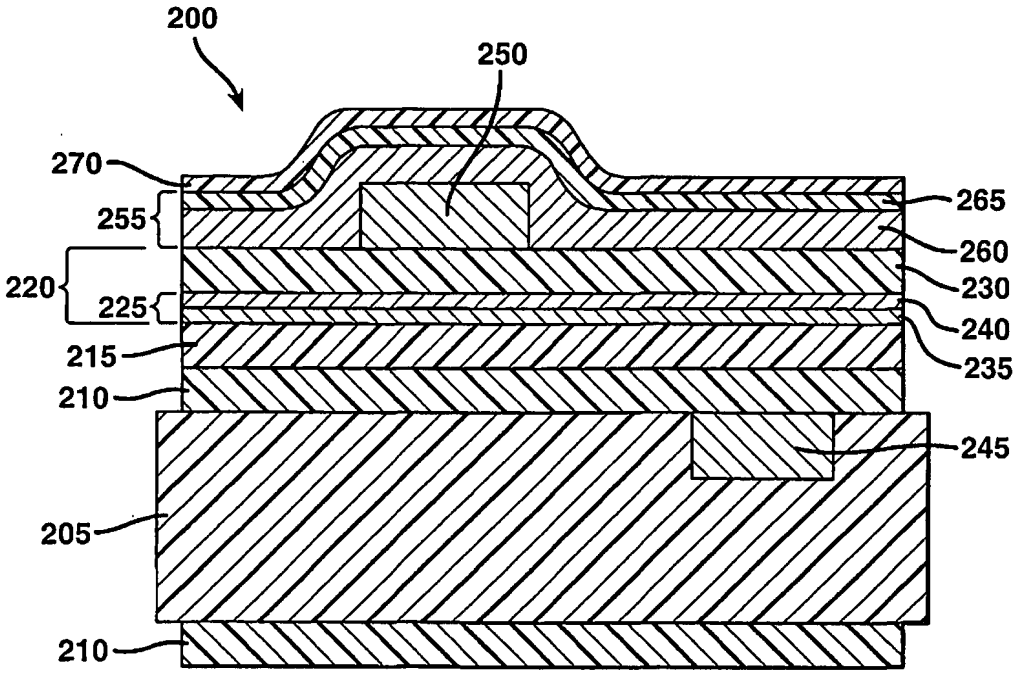
FIG. 2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INTERNATIONAL SEARCH REPORT

Int ial Application No
PCT/US 01/06562

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L51/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 777 281 A (MOTOROLA INC) 4 June 1997 (1997-06-04) the whole document ---	1,17,34, 35,41,42
X	EP 0 977 469 A (HEWLETT PACKARD CO) 2 February 2000 (2000-02-02)	32
A	the whole document ---	1-8,13, 15-19, 34-37, 41-43, 47-50

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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'O' document referring to an oral disclosure, use, exhibition or other means

'P' document published prior to the international filing date but later than the priority date claimed

'T' later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

'X' document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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'&' document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 July 2001	27/07/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	De Laere, A

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INTERNATIONAL SEARCH REPORT

In nal Application No
PCT/US 01/06562

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	WO 00 26973 A (BRIGHT CLARK I ;DELTA V TECHNOLOGIES INC (US)) 11 May 2000 (2000-05-11) abstract	1-7,13, 15-19, 26,27, 32,34
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A	 the whole document	1-7,13, 15-17, 34-37, 41-43, 47-50

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